UNIVERSITY OF DETROIT MERCY  
EE265 - DIGITAL LOGIC CIRCUITS LABORATORY (1:0:3)  
Term 2, 2006-2007

**Course Description:** (Corequisite: EE264) Design and implementation of combinational and sequential logic circuits including counters, adders, shift registers, etc. Computer simulation of logic circuits.

**Instructor:** Dr. Nizar Al-Holou, E330, 993-3365 (phone), alholoun@udmercy.edu

**Office Hours:** Monday: 1-4, Tuesday/Thursday: 1-3 PM, and anytime my office door is open; or email/call to schedule an appointment.

**Class Meetings:** 3:25-6:25 PM, R, E340

**Required Texts:** EE264 text

**Web Site:** [http://knowledge.udmercy.edu](http://knowledge.udmercy.edu)  
This web will have important announcements and other resources will be available here. This page should be consulted frequently, since updates are made regularly. Note in particular that the site has an electronic discussion feature that allows you to ask and answer questions about the course.

**Learning Outcomes:**  
Upon the successful completion of this course, you will be able to:

- Predict the behavior of simple combinational logic circuits, given logic or wiring diagram.
- design and implement simple combinational logic circuits, using gate-level and MSI TTL logic chips
- design and implement simple sequential logic circuits such as counters /shift registers using flip-flops and MSI chips.
- use Altera MAX+PLUS II software to simulate combinational and sequential logic circuits to validate design.
- describe simple combinational and sequential circuits using VHDL
- use PLDs to implement different logic circuits (3a, c, d, e, g, k).

**Requirements:**

**Attendance:** Attendance is MANDATORY!! If an emergency should arise, you may arrange a time to make up a lab, provided you notify me, preferably before, in the same day (Proof may be required).

**Pre-lab reports:** Each group will submit a pre-lab report, which is due at the beginning of the lab period the week before the experiment.

**Reports:** Each group will submit a report, which is due at the beginning of the lab period the week after which the experiment was completed. Reports should be prepared using word processing software, such as Word or WordPerfect.

**Project(s):** design project (s) will include an oral presentation (which will be done by the group) and a design report.

**Quizzes:** Two quizzes will take place during the semester. These questions will assess your individual
mastery of the concepts you apply in lab.

**Tentative Grade:** The final grade will be determined from the following components:

<table>
<thead>
<tr>
<th>Component</th>
<th>Percentage</th>
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<tbody>
<tr>
<td>Pre-lab</td>
<td>10%</td>
</tr>
<tr>
<td>Lab reports, peer review &amp; Lab Activities</td>
<td>30%</td>
</tr>
<tr>
<td>Design Project (s)</td>
<td>20%</td>
</tr>
<tr>
<td>Quizzes</td>
<td>40%</td>
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Note: The peer evaluation will be completed anonymously on the last day. Each team member will rate every other teammate on his/her contribution to the group. The form containing the items on the survey will be available on the web site.

The grading scale for the course is as follows:

- A 93-100, A- 89-92, B+ 85-88, B 80-84, B- 75-79,
- C+ 70-74, C 65-69, C- 60-64, D+ 55-59, D 50-54, F 0-49

**Tentative Laboratory Experiments and Projects:**

1. TTL SSI integrated circuits to implement simple combinatorial logic circuits designs.
2. Combinatorial Logic Circuit Design using SSI
3. Combinatorial Logic Circuit Design using PLA
4. Using VHDL Language to Implement Logic Circuit Design
5. Latches, Flip Flops, and Clocking
6. Counter Design
7. Sequential Circuits Design
8. Design Project (s)